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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,354	07/07/2003	Thomas J. Sonderman	2000.100800	7900

23720 7590 01/13/2005

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,354	THOMAS J. SONDERMAN	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. A new rejection is made as set forth in this Office Action. Claims (1-22) are pending in the application.

Information Disclosure Statement

The Information Disclosure Statement filed on November 22nd, 2004 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Cappelletti et al. (U.S. Patent 5,793,675).

In re claims 1, 9, and 16, **Cappelletti** discloses a method, comprising: performing at least one electrical test (i.e., threshold voltage…) on at least one semiconductor device (memory device, transistor) (col. 3, lines 12-46); determining at least one parameter (i.e., temperature…) of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed semiconductor device (i.e., memory device, transistor…) based upon electrical data obtained from the at least one electrical test (col.

3, lines 48-59); and performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer on the subsequently formed semiconductor device (memory device, transistor) (col. 5, lines 27 to col. 6, line 16).

In re claims 2 and 10, **Cappelletti** discloses that the semiconductor device is at least one of a flash memory device, an application specific integrated circuit and a microprocessor (col. 2, line 61 to col. 3, line 12).

In re claims 3, 11, and 17, **Cappelletti** discloses that performing the at least one electrical test on the at least one semiconductor device comprises performing the at least one electrical test on the at least one semiconductor device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, a programming cycle time and an erase cycle time (col. 3, lines 16-46).

In re claim 4, **Cappelletti** discloses that the semiconductor device is comprised of at least one transistor that is comprises of a gate insulation layer 4 and a gate electrode 5 positioned above the gate insulation layer (col. 1, lines 18-27 and FIG. 1).

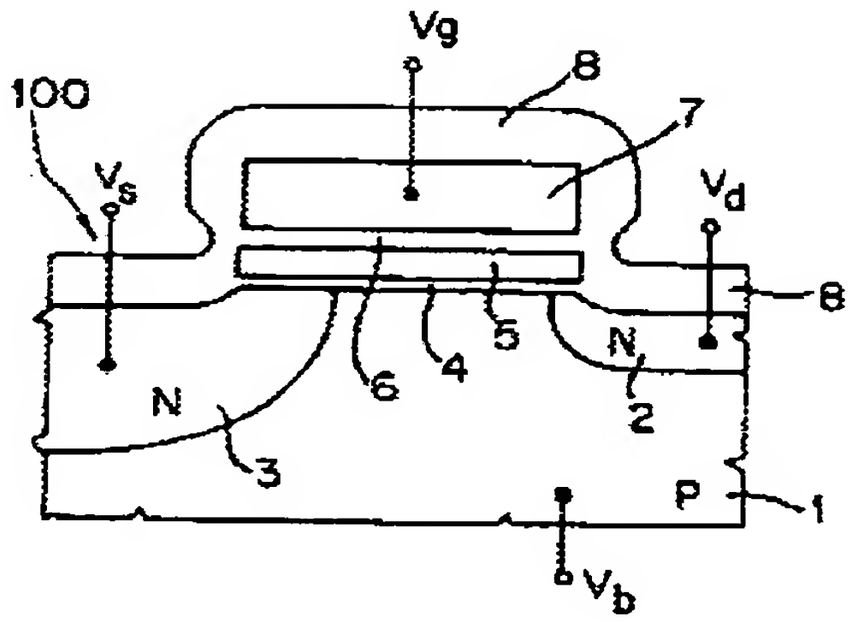

FIG. 1
PRIOR ART

In re claims 5 and 12, **Cappelletti** discloses that the semiconductor device is comprised of a memory device that is comprised of a gate insulation layer 4, a floating gate layer 5 positioned above the gate insulation layer 4, an intermediate insulation layer 6 positioned above the floating gate layer 5, and a control gate layer 7 positioned above the intermediate insulation layer 6 (col. 1, lines 18-27 and FIG. 1).

In re claims 6, 13, and 18, the technique of performing the at least one process operation to form the at least one gate insulation layer on the subsequently formed semiconductor device comprises of at least one of a deposition process and a thermal growth process is well-known to one of ordinary skill in the art at the time of the invention was made.

In re claims 7, 14, and 19, **Cappelletti** discloses that at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting (col. 3, lines 16-59).

In re claims 8, 15, and 20, **Cappelletti** discloses that the gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride (col. 1, lines 18-28).

In re claim 21, **Cappelletti** discloses a method, comprising: performing at least one electrical test on at least one memory device to determine a duration of a programming cycle performed on the memory devices (col. 3, lines 12-46 and col. 4, line 66 to col. 5, line 13); determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon the determined duration of the programming cycle (col. 3,

lines 48-59); and performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer on the subsequently formed memory device (col. 5, lines 27 to col. 6, line 16).

In re claim 22, **Cappelletti** discloses a method, comprising: performing at least one electrical test on at least one memory device to determine a duration of an erase cycle performed on the memory devices (col. 3, lines 12-46 and col. 4, line 66 to col. 5, line 13); determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon the determined duration of the erase cycle (col. 3, lines 48-59); and performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer on the subsequently formed memory device (col. 5, lines 27 to col. 6, line 16).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
January 5th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER